CYPRESS SEMICONDUCTOR

# PAL C 22V10B/PAL C 22V10

## Reprogrammable CMOS PAL® Device

### Features

- Advanced second generation PAL architecture
- Low power
  - 55 mA max "L"
  - 90 mA max standard
  - 120 mA max military
- CMOS EPROM technology for reprogrammability
- Variable product terms
  - 2 × (8 thru 16) product terms
- User programmable macro cell
  - Output polarity control
  - Individually selectable for registered or combinatorial operation
  - "15" commercial & industrial
    10 ns $t_{CO}$
    10 ns $t_S$
    15 ns $t_{PD}$
    50 MHz
  - "20" military
    15 ns $t_{CO}$
    17 ns $t_S$
    20 ns $t_{PD}$
    31 MHz
- Up to 22 input terms and 10 outputs
- Enhanced test features
  - Phantom array
  - Top Test
  - Bottom Test
  - Preload
- High reliability
  - Proven EPROM technology
  - 100% programming and functional testing
- Windowed DIP, windowed LCC, DIP, LCC, PLCC available

### Functional Description

The Cypress PAL C 22V10 is a CMOS second generation Programmable Logic Array device. It is implemented with the familiar sum-of-products (AND-OR) logic structure and a new concept, the "Programmable Macro Cell".

The PAL C 22V10 is executed in a 24 pin 300 mil molded DIP, a 300 mil windowed Cerdip, a 28 lead square ceramic leadless chip carrier, a 28 lead square plastic leaded chip carrier and provides up to 22 inputs and 10 outputs. When the windowed CERDIP is exposed to UV light, the 22V10 is erased and then can be reprogrammed. The Programmable Macro Cell provides the capability of defining the architecture of each output individually. Each of the 10 potential outputs may be specified to be "REGISTERED" or "COMBINATORIAL". Polarity of

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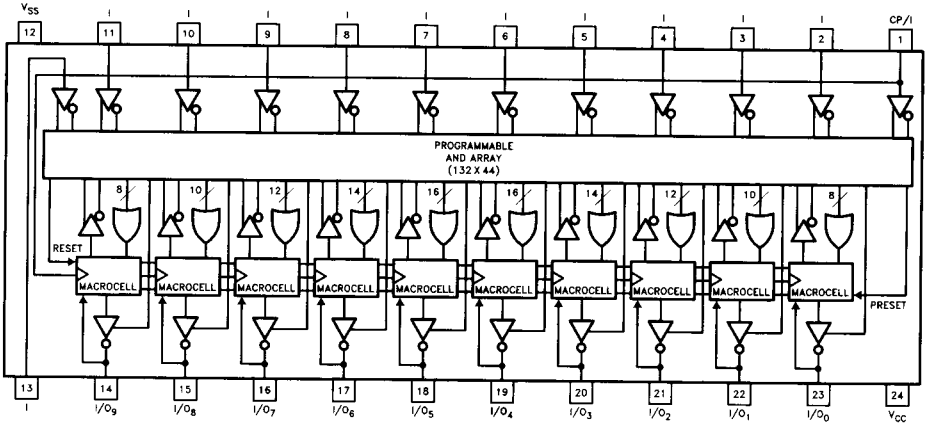
### Logic Symbol and Pinout

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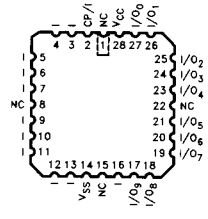
### LCC and PLCC Pinout




0023-10

## Functional Description (Continued)

each output may also be individually selected allowing complete flexibility of output configuration. Further configurability is provided through "ARRAY" configurable "OUTPUT ENABLE" for each potential output. This feature allows the 10 outputs to be reconfigured as inputs on an individual basis or alternately used as a combination I/O controlled by the programmable array.

The PAL C 22V10 features a "VARIABLE PRODUCT TERM" architecture. There are 5 pairs of product terms beginning at 8 product terms per output and incrementing by 2 to 16 product terms per output. By providing this variable structure the PAL C 22V10 is optimized to the configurations found in a majority of applications without creating devices that burden the product term structures with unuseable product terms and lower performance.

Additional features of the Cypress PAL C 22V10 include a synchronous PRESET and an asynchronous RESET product term. These product terms are common to all MACRO CELLS eliminating the need to dedicate standard product terms for initialization functions. The device automatically resets on power-up.

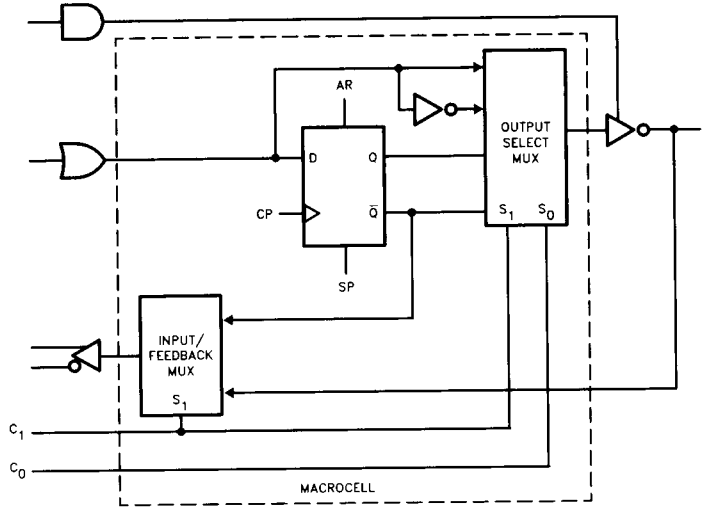
The PAL C 22V10 featuring programmable macro cells and variable product terms provides a device with the flexibility to implement logic functions in the 500 to 800 gate array complexity. Since each of the 10 output pins may be individually configured as inputs on a temporary or permanent basis, functions requiring up to 21 inputs and only a single output down to 12 inputs and 10 outputs are possible. The 10 potential outputs are enabled through the use of product terms. Any output pin may be permanently selected as an output or arbitrarily enabled as an output and an input through the selective use of individual product terms associated with each output. Each of these outputs is achieved through an individual programmable macro cell. These macro cells are programmable to provide a combinatorial or registered inverting or non-inverting output. In a registered mode of operation, the output of the register is fed back into the array providing current status information to the array. This information is available for establishing the next result in applications such as control-state-machines. In a combinatorial configuration, the combinatorial output or, if the output is disabled, the signal present on the I/O pin is made available to the array. The flexibility provided by both programmable macro cell product term control of the outputs and variable product terms allows a significant gain in functional density through the use of programmable logic.

Along with this increase in functional density, the Cypress PAL C 22V10 provides lower power operation thru the use of CMOS technology, increased testability with a register preload feature and guaranteed AC performance through the use of a phantom array. This phantom array ($P_0$–$P_3$) and the "TOP TEST" and "BOTTOM TEST" features allow the 22V10 to be programmed with a test pattern and tested prior to shipment for full AC specifications without using any of the functionality of the device specified for the product application. In addition, this same phantom array may be used to test the PAL C 22V10 at incoming inspection before committing the device to a specific function through programming. PRELOAD facilitates testing programmed devices by loading initial values into the registers.

## Configuration Table 1

| Registered/Combinatorial | | |
|---|---|---|
| $C_1$ | $C_0$ | Configuration |
| 0 | 0 | Registered/Active Low |
| 0 | 1 | Registered/Active High |
| 1 | 0 | Combinatorial/Active Low |
| 1 | 1 | Combinatorial/Active High |

## Macrocell

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## Selection Guide

| Generic Part Number | $I_{CC1}$ mA | | | $t_{PD}$ ns | | $t_S$ ns | | $t_{CO}$ ns | |
|---|---|---|---|---|---|---|---|---|---|
| | "L" | Com/Ind | Mil | Com/Ind | Mil | Com/Ind | Mil | Com/Ind | Mil |
| 22V10B-15 | | 90 | — | 15 | — | 10 | — | 10 | — |
| 22V10B-20 | — | — | 100 | — | 20 | — | 17 | — | 15 |
| 22V10-20 | | 90 | — | 20 | — | 12 | — | 12 | — |
| 22V10-25 | 55 | 90 | 100 | 25 | 25 | 15 | 18 | 15 | 15 |
| 22V10-30 | | — | 100 | — | 30 | — | 20 | — | 20 |
| 22V10-35 | 55 | 90 | — | 35 | — | 30 | — | 25 | — |
| 22V10-40 | | — | 100 | — | 40 | — | 30 | — | 25 |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) ..... 16 mA

UV Exposure ..... 7258 Wsec/cm²

DC Programming Voltage
PAL C 22V10B ..... 13.0V
PAL C 22V10 ..... 14.0V

Latchup Current ..... >200 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +75°C | 5V ±10% |
| Military[6] | −55°C to +125°C | 5V ±10% |
| Industrial | −40°C to +85°C | 5V ±10% |

## Electrical Characteristics Over Operating Range[5]

| Parameters | Description | Test Conditions | | | Min. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH1}$ | Output HIGH Voltage | $V_{CC}$ = Min., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −3.2 mA | COM'L/IND | 2.4 | | V |
| | | | $I_{OH}$ = −2 mA | MIL | | | |
| $V_{OH2}$ | HIGH Level CMOS Output Voltage[3] | $V_{CC}$ = Min., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −100 μA | | $V_{CC}$ − 1.0V | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 16 mA | COM'L/IND | | 0.5 | V |
| | | | $I_{OL}$ = 12 mA | MIL | | | |
| $V_{IH}$ | Input HIGH Level | Guaranteed Input Logical HIGH Voltage for All Inputs[1] | | | 2.0 | | V |
| $V_{IL}$ | Input LOW Level | Guaranteed Input Logical LOW Voltage for All Inputs[1] | | | | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | $V_{SS} \le V_{IN} \le V_{CC}$, $V_{CC}$ = Max. | | | −10 | 10 | μA |
| $I_{OZ}$ | Output Leakage Current | $V_{CC}$ = Max., $V_{SS} \le V_{OUT} \le V_{CC}$ | | | −40 | 40 | μA |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = Max., $V_{OUT}$ = 0.5V[2, 3] | | | −30 | −90 | mA |
| $I_{CC1}$ | Standby Power Supply Current | $V_{CC}$ = Max., $V_{IN}$ = GND Outputs Open for Unprogrammed Device | | "L" | | 55 | mA |
| | | | | COM'L/IND | | 90 | mA |
| | | | | MIL | | 100 | mA |
| | | | | MIL-20 | | 100 | mA |
| $I_{CC2}$ | Operating Power Supply Current | $f_{toggle}$ = $F_{MAX}$[3] Device Programmed with Worst Case Pattern, Outputs Tristated | | COM'L/IND-15 | | 90 | mA |
| | | | | MIL-20 | | 100 | mA |

**Notes:**

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. $V_{OUT}$ = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
3. Tested initially and after any design or process changes that may affect these parameters.
4. *Figure 1a* test load used for all parameters except $t_{EA}$, $t_{ER}$, $t_{PZX}$ and $t_{PXZ}$. *Figure 1b* test load used for $t_{EA}$, $t_{ER}$, $t_{PZX}$ and $t_{PXZ}$.
5. See the last page of this specification for Group A subgroup testing information.
6. $T_A$ is the "instant on" case temperature.

## Capacitance[3]

| Parameters | Description | Test Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1 MHz | | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1 MHz | | 10 | pF |

## Switching Characteristics PAL C 22V10[4, 5]

| Parameters | Description | Commercial & Industrial | | | | | | | | Military | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | B-15 | | -20 | | -25 | | -35 | | B-20 | | -25 | | -30 | | -40 | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PD}$ | Input to Output Propagation Delay[13] | | 15 | | 20 | | 25 | | 35 | | 20 | | 25 | | 30 | | 40 | ns |
| $t_{EA}$ | Input to Output Enable Delay | | 15 | | 20 | | 25 | | 35 | | 20 | | 25 | | 25 | | 40 | ns |
| $t_{ER}$ | Input to Output Disable Delay[8] | | 15 | | 20 | | 25 | | 35 | | 20 | | 25 | | 25 | | 40 | ns |
| $t_{CO}$ | Clock to Output Delay[14] | | 10 | | 12 | | 15 | | 25 | | 15 | | 15 | | 20 | | 25 | ns |
| $t_S$ | Input or Feedback Setup Time | 10 | | 12 | | 15 | | 30 | | 17 | | 18 | | 20 | | 30 | | ns |
| $t_H$ | Input Hold Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_P$ | External Clock Period ($t_{CO}$ + $t_S$) | 20 | | 24 | | 30 | | 55 | | 32 | | 33 | | 40 | | 55 | | ns |
| $t_{WH}$ | Clock Width HIGH[3] | 6 | | 10 | | 12 | | 17 | | 12 | | 14 | | 16 | | 22 | | ns |
| $t_{WL}$ | Clock Width LOW[3] | 6 | | 10 | | 12 | | 17 | | 12 | | 14 | | 16 | | 22 | | ns |
| $f_{MAX1}$ | External Maximum Frequency ($1/(t_{CO} + t_S)$)[9] | 50.0 | | 41.6 | | 33.3 | | 18.1 | | 31.2 | | 30.3 | | 25.0 | | 18.1 | | MHz |
| $f_{MAX2}$ | Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[3, 10] | 83.3 | | 50.0 | | 41.6 | | 29.4 | | 41.6 | | 35.7 | | 31.2 | | 22.7 | | MHz |
| $f_{MAX3}$ | Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[11] | 80.0 | | 45.4 | | 35.7 | | 20.8 | | 33.3 | | 32.2 | | 28.5 | | 20.0 | | MHz |
| $t_{CF}$ | Register Clock to Feedback Input [12] | | 2.5 | | 10 | | 13 | | 18 | | 13 | | 13 | | 15 | | 20 | ns |
| $t_{AW}$ | Asynchronous Reset Width | 15 | | 20 | | 25 | | 35 | | 20 | | 25 | | 30 | | 40 | | ns |
| $t_{AR}$ | Asynchronous Reset Recovery Time | 10 | | 20 | | 25 | | 35 | | 20 | | 25 | | 30 | | 40 | | ns |
| $t_{AP}$ | Asynchronous Reset to Registered Output Delay | | 20 | | 25 | | 25 | | 35 | | 25 | | 25 | | 30 | | 40 | ns |
| $t_{SPR}$ | Synchronous Preset Recovery Time | 10 | | 20 | | 25 | | 35 | | 20 | | 25 | | 30 | | 40 | | ns |
| $t_{PR}$ | Power Up Reset Time[15] | 1.0 | | 1.0 | | 1.0 | | 1.0 | | 1.0 | | 1.0 | | 1.0 | | 1.0 | | μs |

**Notes:**

7. This parameter is sample tested periodically with the device clocked at $f_{MAX}$ external ($f_{MAX1}$) with all registers cycling on each cycle and outputs disabled (in high Z state).
8. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous high level has fallen to 0.5 volts below $V_{OH}$ Min. or a previous low level has risen to 0.5 volts above $V_{OL}$ Max. Please see *Figure 4* for enable and disable test waveforms and measurement reference levels.
9. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feed back can operate.
10. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
11. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feed back can operate. This parameter is tested periodically by sampling production product.
12. This parameter is calculated from the clock period at $f_{MAX}$ internal ($1/f_{MAX3}$) as measured (see note 11 above) minus $t_S$.
13. This specification is guaranteed for all device outputs changing state in a given access cycle. See *Figure 3* for the minimum guaranteed negative correction which may be subtracted from $t_{PD}$ for cases in which fewer outputs are changing state per access cycle.
14. This specification is guaranteed for all device outputs changing state in a given access cycle. See *Figure 3* for the minimum guaranteed negative correction which may be subtracted from $t_{CO}$ for cases in which fewer outputs are changing state per access cycle.
15. The registers in the PAL C 22V10 have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in $V_{CC}$ must be monotonic and the timing constraints depicted in *Figure 5* must be satisfied.
16. The clock signal input must be in a valid LOW state ($V_{IN}$ less than 0.8V) or a valid HIGH state ($V_{IN}$ greater than 2.4V) prior to occurrence of the 10% level on the monotonically rising power supply voltage as shown in *Figure 5*. In addition, the clock input signal must remain stable in that valid state as indicated until the 90% level on the power supply voltage has been reached. The clock signal may transition LOW to HIGH to clock in new data or to execute a synchronous preset after the indicated delay ($t_{PR}$ + $t_S$) has been observed.

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## AC Test Loads and Waveforms (Commercial)

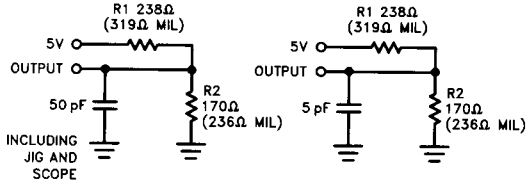



**Figure 1a** **Figure 1b**

0023-11

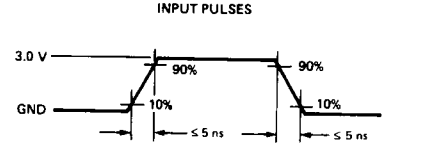
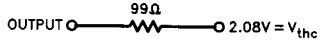



**Figure 2**

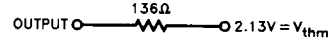
0023-12

Equivalent to: THÉVENIN EQUIVALENT (Commercial)



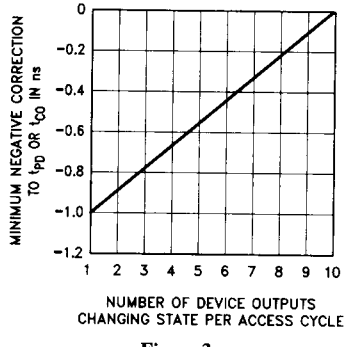

0023-13

Equivalent to: THÉVENIN EQUIVALENT (Military)




0023-14

**Minimum Negative Correction to $t_{PD}$ and $t_{CO}$ vs. Number of Outputs Switching**




0023-20

**Figure 3**

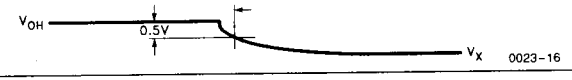
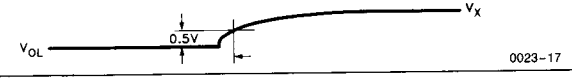
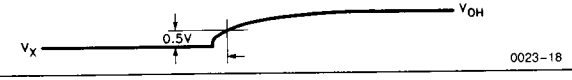
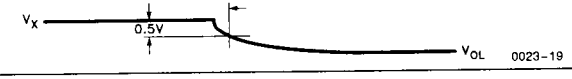
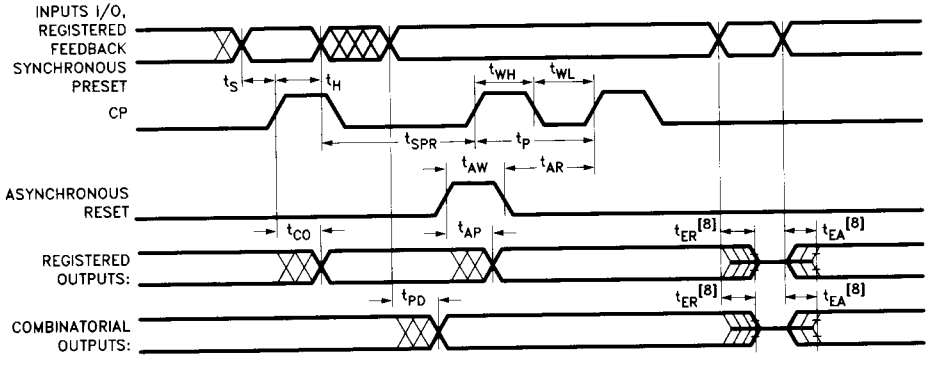
| Parameter | $V_X$ | Output Waveform—Measurement Level |
|---|---|---|
| $t_{ER(-)}$ | 1.5V |  |
| $t_{ER(+)}$ | 2.6V |  |
| $t_{EA(+)}$ | $V_{thc}$ |  |
| $t_{EA(-)}$ | $V_{thc}$ |  |



**Figure 4. Test Waveforms**

## Switching Waveform




## Power-Up Reset Waveform[15, 16]

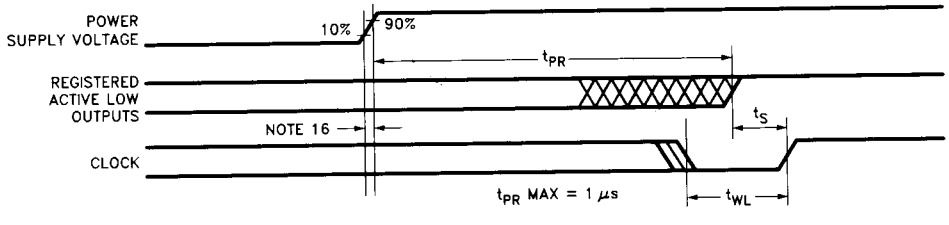
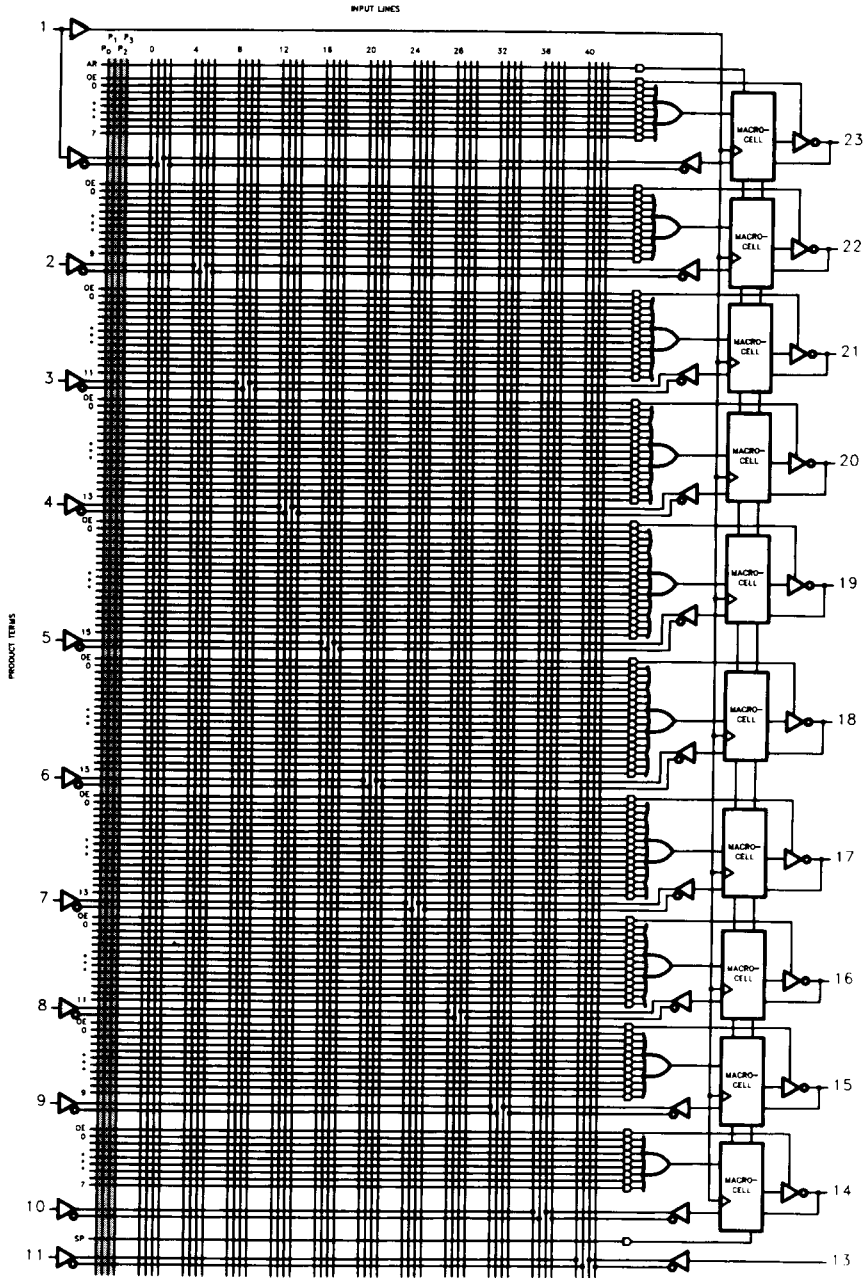



**Figure 5**

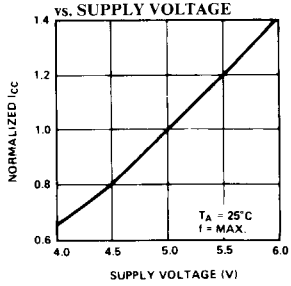
## Functional Logic Diagram PAL C 22V10



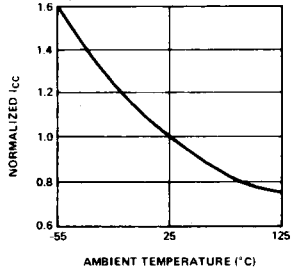

0023-4

## Typical DC and AC Characteristics

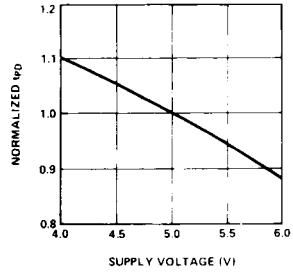
NORMALIZED STANDBY SUPPLY CURRENT ($I_{CC1}$) vs. SUPPLY VOLTAGE



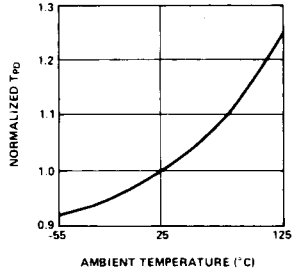

NORMALIZED STANDBY SUPPLY CURRENT ($I_{CC1}$) vs. AMBIENT TEMPERATURE



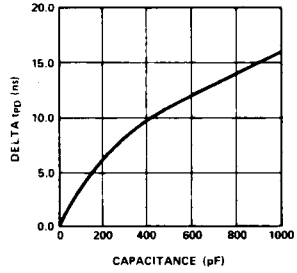

NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE



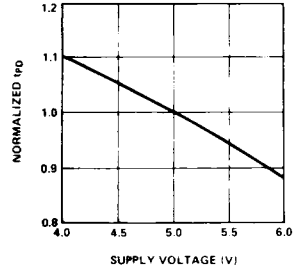

NORMALIZED PROPAGATION DELAY vs. TEMPERATURE



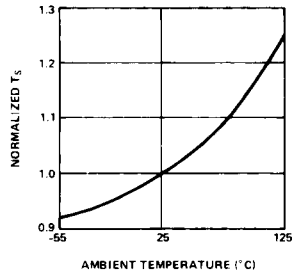

DELTA PROPAGATION TIME vs. OUTPUT LOADING



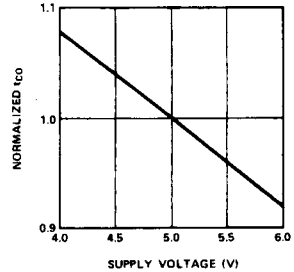

NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE



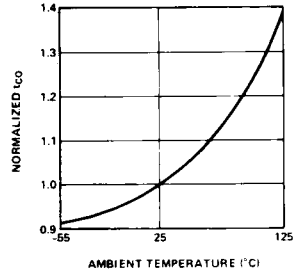

NORMALIZED SETUP TIME vs. TEMPERATURE



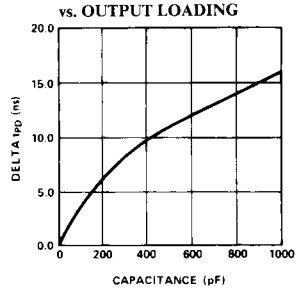

NORMALIZED CLOCK TO OUTPUT TIME vs. SUPPLY VOLTAGE



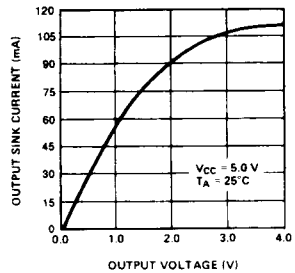

NORMALIZED CLOCK TO OUTPUT TIME vs. TEMPERATURE



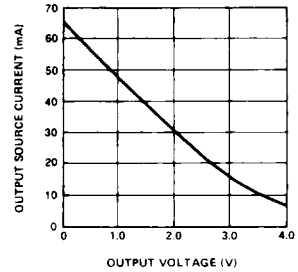

DELTA CLOCK TO OUTPUT TIME vs. OUTPUT LOADING




OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE




OUTPUT SOURCE CURRENT vs. VOLTAGE




0023-15

## Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the PAL C 22V10. For this reason, an opaque label should be placed over the window if the device is exposed to sunlight or fluorescent lighting for extended periods of time. In addition, high ambient light levels can create hole-electron pairs which may cause "blank" check failures or "verify errors" when programming "windowed" parts. This phenomenon can be avoided by use of an opaque label over the window during programming in high ambient light environments.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity $\times$ exposure time) of 25 Wsec/cm$^2$. For an ultraviolet lamp with a 12 mW/cm$^2$ power rating, the exposure would be approximately 35 minutes. The PAL C 22V10 needs to be placed within 1 inch of the lamp during erasure. Permanent damage may result if the device is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm$^2$ is the recommended maximum dosage.

## Ordering Information

| $I_{CC}$ (mA) | $t_{PD}$ (ns) | $t_S$ (ns) | $t_{CO}$ (ns) | Ordering Code | Package | Operating Range |
|---|---|---|---|---|---|---|
| 90 | 15 | 10 | 10 | PAL C 22V10B-15PC/PI | P13 | Commercial/Industrial |
| | | | | PAL C 22V10B-15WC/WI | W14 | |
| | | | | PAL C 22V10B-15JC/JI | J64 | |
| | | | | PAL C 22V10B-15HC | H64 | |
| 90 | 20 | 12 | 12 | PAL C 22V10-20PC/PI | P13 | Commercial/Industrial |
| | | | | PAL C 22V10-20WC/WI | W14 | |
| | | | | PAL C 22V10-20JC/JI | J64 | |
| | | | | PAL C 22V10-20HC | H64 | |
| 120 | 20 | 17 | 15 | PAL C 22V10B-20DMB | D14 | Military |
| | | | | PAL C 22V10B-20WMB | W14 | |
| | | | | PAL C 22V10B-20HMB | H64 | |
| | | | | PAL C 22V10B-20LMB | L64 | |
| | | | | PAL C 22V10B-20QMB | Q64 | |
| | | | | PAL C 22V10B-20KMB | K73 | |
| 55 | 25 | 15 | 15 | PAL C 22V10L-25PC | P13 | Commercial |
| | | | | PAL C 22V10L-25WC | W14 | |
| | | | | PAL C 22V10L-25JC | J64 | |
| | | | | PAL C 22V10L-25HC | H64 | |
| 90 | 25 | 15 | 15 | PAL C 22V10-25PC/PI | P13 | Commercial/Industrial |
| | | | | PAL C 22V10-25WC/WI | W14 | |
| | | | | PAL C 22V10-25JC/JI | J64 | |
| | | | | PAL C 22V10-25HC | H64 | |
| 100 | 25 | 18 | 15 | PAL C 22V10-25DMB | D14 | Military |
| | | | | PAL C 22V10-25WMB | W14 | |
| | | | | PAL C 22V10-25HMB | H64 | |
| | | | | PAL C 22V10-25LMB | L64 | |
| | | | | PAL C 22V10-25QMB | Q64 | |
| | | | | PAL C 22V10-25KMB | K73 | |
| 100 | 30 | 20 | 20 | PAL C 22V10-30DMB | D14 | Military |
| | | | | PAL C 22V10-30WMB | W14 | |
| | | | | PAL C 22V10-30HMB | H64 | |
| | | | | PAL C 22V10-30LMB | L64 | |
| | | | | PAL C 22V10-30QMB | Q64 | |
| | | | | PAL C 22V10-30KMB | K73 | |
| 55 | 35 | 30 | 25 | PAL C 22V10L-35PC | P13 | Commercial |
| | | | | PAL C 22V10L-35WC | W14 | |
| | | | | PAL C 22V10L-35JC | J64 | |
| | | | | PAL C 22V10L-35HC | H64 | |
| 90 | 35 | 30 | 25 | PAL C 22V10-35PC/PI | P13 | Commercial/Industrial |
| | | | | PAL C 22V10-35WC/WI | W14 | |
| | | | | PAL C 22V10-35JC/JI | J64 | |
| | | | | PAL C 22V10-35HC | H64 | |
| 100 | 40 | 30 | 25 | PAL C 22V10-40DMB | D14 | Military |
| | | | | PAL C 22V10-40WMB | W14 | |
| | | | | PAL C 22V10-40HMB | H64 | |
| | | | | PAL C 22V10-40LMB | L64 | |
| | | | | PAL C 22V10-40QMB | Q64 | |
| | | | | PAL C 22V10-40KMB | K73 | |

## MILITARY SPECIFICATIONS
### Group A Subgroup Testing

### DC Characteristics

| Parameters | Subgroups |
|---|---|
| $V_{OH}$ | 1,2,3 |
| $V_{OL}$ | 1,2,3 |
| $V_{IH}$ | 1,2,3 |
| $V_{IL}$ | 1,2,3 |
| $I_{IX}$ | 1,2,3 |
| $I_{OZ}$ | 1,2,3 |
| $I_{CC}$ | 1,2,3 |



### Switching Characteristics

| Parameters | Subgroups |
|---|---|
| $t_{PD}$ | 7,8,9,10,11 |
| $t_{CO}$ | 7,8,9,10,11 |
| $t_S$ | 7,8,9,10,11 |
| $t_H$ | 7,8,9,10,11 |

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